IR-1641 (2-1929)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of:

Thomas Herman, et al.

Date: November 14, 2003

Serial No.: 10/044,427

Group Art Unit: 2822

Filed: November 9, 2001

For: MOSFET WITH REDUCED THRESHOLD VOLTAGE AND ON RESISTANCE AND PROCESS FOR ITS MANUFACTURE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF UNDER 37 C.F.R. §1.192

Sir:

This appeal is taken from the Examiner's final rejection dated March 20, 2003, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on July 21, 2003.

I. Status of Claims

Claims 2-8 stand rejected and are pending on appeal.

II. Real Party in Interest

The real party in interest is the assignee, International Rectifier Corporation.

III. Related Appeals and Interferences

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

IV. Status of Amendments

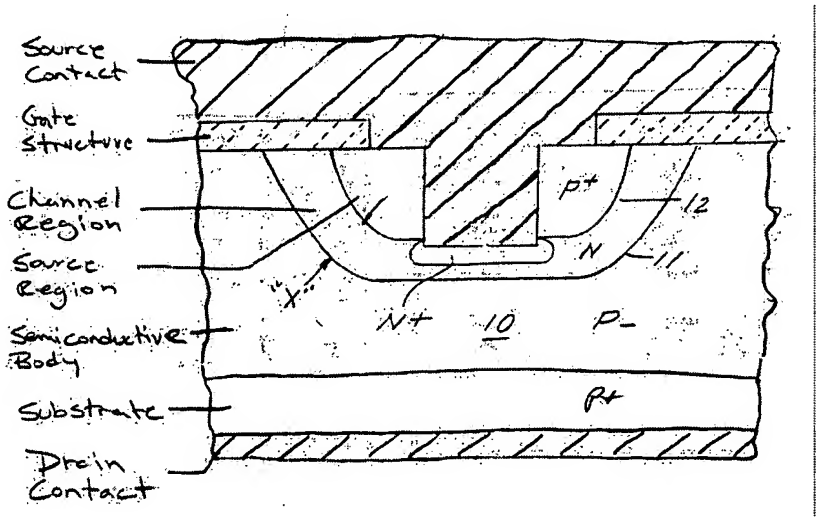
An Amendment/Submission containing arguments regarding the patentability of the claims was filed after the final rejection on June 20, 2003, and was considered.

V. Summary of Invention

The present invention relates to semiconductor power switching devices and more particularly to a planar type power MOSFET.

Power MOSFETs are well known. A planar type power MOSFET is a well known configuration of such devices.

A planar power MOSFET includes a plurality of active cells formed in a common typically monocrystalline semiconductive body such as doped silicon. The Figure below, which is based on Figure 1 from the specification, shows a single cell of a typical planar MOSFET.



A cell of a planar power MOSFET includes a channel region formed in the semiconductive body, a source region formed in the channel region and spaced from the semiconductive body, and a gate structure formed over that portion of the channel region that extends between the semiconductive body and the source region. The semiconductive body may be of P-type or N-type conductivity. In a typical configuration, the semiconductive body is a monocrystalline layer formed through epitaxial growth over a substrate of the same conductivity.

The channel region in a typical cell of a planar power MOSFET is a region of a conductivity opposite to the conductivity of the semiconductive body. The channel region is formed usually through either diffusion of dopants into the semiconductive body, or through implantation and then diffusion of dopants. Diffusion is obtained by application of heat over a desired period of time.

The source region in a typical cell of a planar MOSFET is a region of a conductivity opposite to that of the channel region in which it is formed. Thus, the source region is the same conductivity as the semiconductive body. The source region is smaller in width than the channel region in which it is formed and is thus spaced from the semiconductive body by a region of opposite conductivity. Current can pass between the source region and the semiconductive body if a portion of the region in the channel region that is disposed between the semiconductive body and the source region is converted to be of the same conductivity as the source region and the semiconductive body. To make it so, a portion of the channel region between the source region and the semiconductive body is made to change polarity through what is commonly referred to as inversion. Inversion occurs when an appropriate voltage is applied to the gate structure to cause the formation of a region of opposite conductivity in the channel region thereby allowing the possibility of electrical connection between the source region and the semiconductive body. The inverted region is typically referred to as a channel or an invertible channel.

In a well known power MOSFET, the current in each cell flows from a contact that is electrically connected to the source region through an adjacent respective channel into the semiconductive body and then through a substrate (on which the semiconductive body is formed) into a drain contact that is electrically connected to the substrate. Thus, the path of the current in such devices is vertical between the source contact and the drain contact.

The resistance of a power MOSFET when it is conducting (Rdson) is an important performance characteristic. In low voltage devices, for example under 50 volts, an important indicator is Rdson under low gate to source (Vgs) conditions. A method of reducing Rdson under low Vgs condition is to reduce the threshold voltage (Vth) of the device. Vth is the minimum gate voltage necessary to create a channel. Lowering Vgs ensures that the device is fully ON under low voltage conditions.

V_{th} can be reduced if the length of the channel is reduced. The length of the channel can be reduced if the depth of the channel region is reduced. The depth of the channel can be reduced if the thermal exposure of the channel region is limited during the manufacturing of the device. That is, by minimizing the total heat exposure, or the so called overall thermal budget, the lateral expansion of the channel region as well as its depth can be limited, thereby reducing the channel length (i.e. the portion of channel region beneath the gate structure).

However, when the channel regions are made too shallow (when the thermal budget is kept low) the resulting source regions are more "oblong" (or elongated in depth) in the vertical direction creating a region in the device where the corner of the source region is very near the "corner" (in cross-section) of the channel region. This is marked as X in the Figure (also in Figure 1).

Thus, when the diffusion drive is kept to a minimum in order to keep the depth of the channel region shallow, there is relatively little lateral diffusion of the source junction 12. As a result, the shape of source junction 13 is deeper with less lateral spreading, i.e. more "oblong" than a typical diffused junction. Consequently, dimension "X" is reduced. It has been found that under such circumstances the device is susceptible to an undesirable condition called punch through.

Punch through is a phenomena associated with the merging of the depletion regions of the source region and the drain region. Specifically, under reverse bias, punch through occurs when the depletion region between the channel region and the drain region extends to meet the source region causing unnecessary and unacceptable leakage of current from the drain to the source. When the dimension X is small the chance of punch through is increased.

According to the present invention to retain the benefits of a shallow channel region (low Vth and Rdson) the positions and shapes of the source and channel regions are controlled in order to avoid punch through. Specifically, the depth of the channel region is kept below 3μ and the depth of the source regions are kept to below 0.3μ.

Thus, claims 8 calls for:

> 8. A vertical conduction power MOSFET, comprising:
>
> a die of monocrystaline silicon, said die being of a first conductivity type and having a first and a second surface;
>
> a relatively thin layer of epitaxially grown silicon of said first conductivity type on said first surface;
>
> a plurality of spaced channel regions of a second conductivity type diffused into the surface of said layer of epitaxially grown silicon;
>
> a plurality of respective source diffusion regions of said first conductivity type, each of respective source diffusion regions being diffused into each of said plurality of spaced channel regions and each said respective source diffusion region having a smaller area than each of said plurality spaced channel regions, and defining at least one lateral invertible channel region in a space between its periphery of and its respective channel region;
>
> a MOSgate structure overlying each of said lateral invertible channel regions;
>
> a source electrode overlying a surface of said die and connected to each of said plurality of spaced channel regions and said respective source diffusion regions, and insulated from said MOSgate structure; and
>
> a drain electrode coupled to said layer of epitaxially grown silicon, wherein each of said plurality of spaced channel regions has a depth of less than 3 microns, and each of said respective source diffusion regions has a depth of less than 0.3 microns.

Claim 8 was introduced as a new claim in an amendment dated December 27, 2002. Claim 8 was introduced to replace claim 1 which had been rejected as obvious over Huang, U.S. Patent No. 6,255,692 in view of Lidow et al., U.S. Patent No. 4,680,853.

Huang shows a trench type device. In such devices, the gate structure extends vertically into a channel region and is adjacent a vertically oriented channel.

Lidow et al. show a planar power MOSFET.

In the amendment of December 27th, claim 8 was distinguished over Huang as claiming lateral invertible channel regions, unlike Huang which only shows vertical invertible channel regions:

> The device shown in Huang comprises a trench type device that has vertically oriented invertible channel regions. Unlike the device shown in Huang, a device according to claim 8 comprises a plurality of *lateral invertible* channel regions.

In an Office Action mailed March 20, 2003, Claim 8 was rejected under 35 U.S.C. §103(a) over Huang in view of Lidow et al. In support of the rejection of claim 8 the Examiner stated that Huang discloses the following:

a) a die of monocrystaline silicon (2a) said die being of a first conductivity and having a first and second surface (See Figure 1);

b) a relatively thin layer of epitaxially grown silicon (2) of said first conductivity type on said first surface (See Figure 1);

c) a plurality of spaced channel regions (12) of a second conductivity type diffused into surface of said layer epitaxially grown silicon (See Figure 1);

d) a plurality of respective source diffusion regions (1) of said first conductivity type, each of respective source diffusion regions being diffused into each of said plurality of spaced channel regions and each said respective source diffusion regions having a smaller area than each of said plurality spaced channel regions, and defining at least one lateral invertible channels region in a space between its periphery of and its respective channel region (See Figure 1);

e) a MOSgate structure overlying each of said lateral invertible channel regions (See Figure 1);

f) a source electrode (21) overlying the top of said die and connected to each of said plurality of spaced channel regions and said respective source diffusion regions; and insulated from said MOSgate structure (See Figure 1);

g) a drain electrode (22) coupled to said layer of epitaxially grown silicon (See Figure 1);

h) plurality of spaced channel regions has a depth less then 3 microns, and said source diffusion has a depth less than .3 microns (See Column 6, lines 24-64).

In regards to claim 8, Huang fails to disclose the following:
a) channel region of a second conductivity.

However, Lidow et al. ("Lidow") discloses a channel that has a second conductivity type (See Figure 20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Huang to include a channel that has a second conductivity type as disclosed in Lidow because it aids in decreasing the forward resistance of the MOSFET (See Column 1 Lines 25-48).

In response to the arguments distinguishing claim 8 over the cited art, the Examiner stated that "invertible is defined as capable of being inverted and inverted is defined as to turn inside out or upside down. Therefore, since the channel region is invertible it means that it can be turned upside down in a vertical direction." Office Action, 3/20/2003, Par. 5.

In response to the Examiner's argument the following was argued:

Invertible in the art of MOSgated devices means a region of one conductivity type which can be turned into a region of another conductivity type through inversion. Inversion as is well known in the art occurs upon application of an electric field through for example a gate structure. It is respectfully submitted that a person skilled in the art would not read invertible channel as a channel that can be physically "turned upside down in a vertical direction." Indeed, such is impossible in that channel regions are not capable of physical movement within the device.

The arguments set forth in the response of December 27, 2002 were meant to point out that Huang teaches a device with vertically oriented channel regions. On the other hand, claim 8 is directed at a planar device which include laterally extending channel regions. The teachings of Huang including the dimensions disclosed therein for source regions and the channel region do not apply to planar devices. In planar devices, the depth of the source region contained within the channel region has a bearing on the characteristics of the device. Most notable of such characteristics is the ability of the device to withstand punch through. As explained in the background of the application when the source region is made too deep the distance between its outer boundary and the junction between the body in which the source region is contained, and the drain region in which the body region is contained (the distance being designated as X in Figure 1) has a

direct effect on the ability of the device to withstand punch through during reverse bias conditions. Thus, to increase the distance between the outer boundary of source regions and the junction between the body region and the drain (distance X, Figure 1), the thermal treatment step during the processing of conventional devices is limited to prevent the outer boundary of the source regions from approaching the junction of the body region and the drain region. As a result of a limited thermal step, the source regions do not advance deeper within the body regions in which they are contained, and more importantly do not advance laterally either. Thus, in prior art devices there was a limitation on how short the channel could be made in order to improve the capability of the device to withstand punch through. Of course, the longer the channel, the higher such characteristics as V_{th} and Rdson (ON resistance).

According to the present invention, the source regions are made extremely shallow (less than 0.3 microns as called for by claim 8). As a result punch through can be limited. See specification, page 6, paragraph 22. There is no disclosure in Huang or any other cited reference, which teaches or suggests making the source regions in a planar device of such dimensions in order to improve the ability of the device to withstand punch through. Accordingly, it is respectfully submitted that the subject matter of claim 8 is not obvious over Huang in view of Lidow. (Emphasis added).

In an Advisory Action dated July 18, 2003, the Examiner only stated the following:

Applicant argues that "there is no disclosure in Huang or any other cited reference, which teaches or suggests making the source regions in a planar device of such dimensions in order to improve the ability of the device to withstand punch through." However, Huang discloses a source region that is less than .3 microns (For Example: See Column 6 Lines 24-64).

VI. Issues on Appeal

Whether claims 2-8 are obvious under 35 U.S.C. 103 (a) over Huang in view of Lidow et al.

VII. Grouping of Claims

Claims 2-8 stand or fall together.

VIII. Argument

First, claim 8 calls for lateral invertible channels. The Examiner has stated that Huang shows lateral invertible channels. Huang, however, shows a trench type device. Such devices include vertically oriented channel regions adjacent to the gate structures. The Examiner's assertion is, therefore, clearly erroneous.

Moreover, the Examiner has not cited any teaching or suggestion in Huang or any other cited art that would motivate a person skilled in the art to change the device of Huang to a planar device having lateral invertible channels.

The Examiner has cited Lidow et al. as showing a channel region of a second conductivity type and argued that Huang could be modified to include such a channel region because it aids in decreasing the forward resistance of the MOSFET.

It is submitted that the channel region in Huang is of the second conductivity. That is, it is of a conductivity opposite to the silicon body (region 2 in Huang) in which it is formed. This is the case with all channel regions in MOSFETs of any type. Thus, the suggested modification to Huang by Lidow et al. would not change the device into anything different. Furthermore, it has not been established how the teachings of Lidow et al. could reduce the resistance of the device shown by Huang.

Second, Huang does not teach a person skilled in the art to devise a planar device having diffused source regions that are 0.3 microns deep in that the values recited in Huang are relevant and applicable only to a heterojunction between silicon and silicon germanium.

Claim 8 calls for, in combination with other limitations, a plurality of spaced channel regions and a plurality of respective source diffusion regions diffused into each of the plurality of spaced channel regions, the "plurality of spaced channel regions [having] a depth of less than 3 microns, and each of said respective source diffusion regions [having] a depth of less than 0.3 microns".

The channel regions of claim 8 are defined to be "diffused" into the surface of a monocrystalline, epitaxially grown silicon. The channel regions are, therefore, formed in a silicon body. Furthermore, because the source regions are diffused into the channel regions, they

too are formed in a silicon body. Claim 8, therefore, calls for a structurally different device that is not taught or suggested by the cited art.

Specifically, claim 8 calls for diffused source and channel regions of the same material, namely, silicon. Thus, in a device according to claim 8, a homojunction is formed by each source region and channel region.

On the other hand, Huang teaches a heterojunction between the source region and the channel region. The thickness of the source region in Huang is necessitated by the fact that Huang requires a heterojunction. Thus, the teaching of Hunag could not be applicable to a planar device in which the source regions and the channel regions form homojunctions as explained below.

Huang shows a trench type MOSFET which includes a channel region 3, and source regions 1 (See Fig. 1 as an example). According to Huang, source regions 1 are formed from a narrow-band gap material. The narrow-band gap material is dissimilar from the material in which the channel region 3 is formed. The reason for using a narrow-band gap material for forming the source regions is to form a heterojunction (a junction between two dissimilar materials) in order to avoid having a parasitic element, namely a parasitic transistor, turned on under a reverse bias condition, thereby improving the "ruggedness" of the device. Huang summarizes the problem that his invention intends to address and the solution to the problem in Col. 1, line 1-Col. 2, line 27. A salient passage from Huang summarizing his teaching is provided below:

> The narrow-bandgap material in this power device is doped to provide these source regions which form with the body regions a source p-n junction that comprises the heterojunction. This p-n heterojunction serves to suppress so-called "second breakdown", which would otherwise result from the turning on of a parasitic bipolar transistor (formed by the body region of the first conductivity type between the first source and second regions of the second conductivity type) in a high-current high-voltage condition between the first main electrode and the second region. This improves the safe operating area (SOA) of the power device, also termed its "ruggedness". Col. 1, lines 60-66.

Now referring to the specification of Huang, the narrow-band gap material used to form the source regions is silicon germanium, which is deposited over the top surface of a silicon body in which the channel region is formed.

> Because it is a layer 11 deposited on a major surface 10a of the semiconductor body 10, this narrow-bandgap source region 1 is outside the semiconductor body 10, and the resulting, combined p-n heterojunction 31 is formed at the body surface 10a. Col. 3, lines 20-24. (Emphasis added.)

It should be noted that the channel region 3 is formed in an epitaxial monocrystalline silicon layer:

> The Si body region 3 may be an epitaxial layer deposited on the monocrystalline Si region 2 with a uniform doping concentration (P), or it may be s[sic] formed with a graded doping concentration (P) by implantation overdoping in the region 2. Col. 6, lines 44-48.

Huang states that the silicon germanium layer is an epitaxial layer (formed by epitaxial growth) to a thickness of between 10nm-50nm.

> The source region 1 may be simply a single thin epitaxial layer 11 of $Si_xGe_{(1-x)}$ having a thickness in the range of, for example, 10 nm (nanometers) to 50nm. Col. 6, lines 24-26.

The thickness of the silicon germanium is a factor in the construction of the device shown by Huang as there may be strain between the germanium based crystal and the silicon crystal over which the silicon germanium is formed. To be specific, Huang teaches controlling the thickness of the silicon germanium crystal to avoid adverse consequences that may result from "lattice mismatch" at the heterojunction of silicon germanium and the silicon in which the channel region is formed.

> The proportion (1-x) of Ge in this alloy layer 11 is chosen sufficiently high to provide the additional potential energy barrier required at the p-n junction 31 to give the desired injection ratios between the regions 1 and 3, without the crystal lattice at the heterojunction 31 being damaged by strain due to the lattice mismatch of Ge with Si. Col. 6, lines 27-34.

The atoms that form a crystalline substance such as a semiconductor material are regularly arranged in three dimensional lattices. When two dissimilar crystalline substances are joined together, the differences between their lattice dimensions cause stress. The stress causes a deformation in the lattice of one or both materials which if great may cause the failure of the junction between the two materials. This is the problem of lattice mismatch which is addressed by Huang. That is Huang teaches that the differences in the lattice dimension between silicon and silicon germanium may cause a strain at the heterojunction which can be avoided by having silicon germanium formed at a proper thickness.

Thus, thickness is a factor in the device shown by Huang because silicon germanium is being used as a material for the source region, while the channel region is formed in a silicon body. Otherwise, thickness of the source region is not taught to be of independent significance.

It is submitted that Huang does not lead a person skilled in the art to construct a planar device to have diffused source regions that are 0.3 microns deep because the thickness of the source regions in Huang are dictated by the fact that Huang's source regions are formed from a material different from the material in which the channel region is formed. Where that is not the case, the problem of lattice mismatch does not exist (because the source region and the channel region are formed in the same material), and therefore the teaching of Huang as to the proper thickness of the source region is irrelevant. It is submitted that one skilled in the art would not use the values recited in Huang in constructing a device having source regions that are diffused into the channel region as is the case with claim 8. Therefore, Huang does not teach a person skilled in the art to modify a planar MOSFET to have diffused source regions that are less than 0.3 microns deep.

Third, the teaching of Huang as to the values for the thickness of the source region is not applicable to devices that include diffused source regions because a deposited source, like the one in Huang, cannot solve the problem of punch-through, which exists when the source regions are diffused into channel regions.

In order to form the source regions, Huang teaches epitaxially growing silicon germanium over silicon in which the channel region is formed. The problem of punch through in planar devices is due to the fact that the boundary of the source region approaches the boundary of

channel region when the source region is diffused into the channel region. However, when source regions are grown epitaxially the problem of punch through is not an important design factor because the source regions are not approaching the boundary of the channel. Quite simply, through epitaxial growth, source regions in the device shown by Huang vertically grow over and above the surface of the channel region; the source regions do not penetrate into the channel region. Whereas, diffusion leads to the extension of the source region into the body of the channel region which results in the source region approaching the junction between the channel region and the semiconductive body in which it is formed. Huang, which teaches forming source regions of shallow thickness by epitaxial growth, does not actually provide a process which produces a structure that can provide a solution that is related to the problem addressed by the invention. Thus, Huang cannot be applied to solve the problems addressed by the present invention.

Last, Huang teaches epitaxially grown source regions which are of a different material from the material in which the channel region is formed. Specifically, the source regions in Huang are made from Silicon Germanium while the channel region is composed of monocrystalline Silicon. Thus, for the sake of argument, if Huang is modified to become a planar device the result is a device that includes source regions made of a different material in which the channel is formed. This is not the case with Claim 8.

In short, Huang does not teach or suggest modifying a planar device to have diffused source regions that are 0.3 microns deep and have channel regions that are less than 3 microns as called for by claim 8.

Claims 2-7 depend from claim 8 and, therefore, include its limitations. Each of these claims includes other limitations which in combination with those of claim 8 are not shown or suggested by the art of record. Claims 2-7 should, therefore, be deemed allowable.

IX. Conclusion

Claims 2-8 are not obvious under 35 U.S.C. §103(a) over Huang in view of Lidow et al.

Our check No. 13227, which includes the amount of $330 to cover the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37

C.F.R. 1.192 and applicant reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing the required papers by the number of months which will avoid abandonment under 37 C.F.R §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

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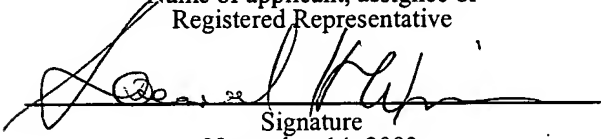

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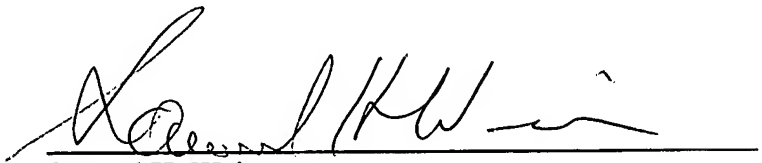
November 14, 2003

Date of Signature

Respectfully submitted,



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APPENDIX OF CLAIMS ON APPEAL

2. The MOSFET of claim 8, wherein said first and second conductivity types are N and P respectively.

3. The MOSFET of claim 8, wherein said lateral invertible channels have a length of less than about 1 microns, whereby the distance between respective pairs of said source and channel regions at their corner points of maximum curvature is about 2.5 microns.

4. The MOSFET of claim 8, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

5. The MOSFET of claim 2, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

6. The MOSFET of claim 3, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

7. The MOSFET of claim 5, wherein said first concentration type is N and wherein said high concentration contact diffusion is a phosphorus diffusion formed with an effective implant energy of greater than about 350 keV for a singly charged phosphorous ion.

8. A vertical conduction power MOSFET, comprising:

a die of monocrystaline silicon, said die being of a first conductivity type and having a first and a second surface;

a relatively thin layer of epitaxially grown silicon of said first conductivity type on said first surface;

a plurality of spaced channel regions of a second conductivity type diffused into the surface of said layer of epitaxially grown silicon;

a plurality of respective source diffusion regions of said first conductivity type, each of respective source diffusion regions being diffused into each of said plurality of spaced channel regions and each said respective source diffusion region having a smaller area than each of said plurality spaced channel regions, and defining at least one lateral invertible channel region in a space between its periphery of and its respective channel region;

a MOSgate structure overlying each of said lateral invertible channel regions;

a source electrode overlying a surface of said die and connected to each of said plurality of spaced channel regions and said respective source diffusion regions, and insulated from said MOSgate structure; and

a drain electrode coupled to said layer of epitaxially grown silicon, wherein each of said plurality of spaced channel regions has a depth of less than 3 microns, and each of said respective source diffusion regions has a depth of less than 0.3 microns.